



INFORMATION DISCLOSURE CITATION  
(Use several sheets if necessary)

ATTY DOCKET NO. ITO.0047US (P16202) SERIAL NO. 10/633,874  
APPLICANT(S): BRIAN G. JOHNSON  
FILING DATE: August 4, 2003 GROUP ART UNIT:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
A.		5,166,758	11/24/1992	OVSHINSKY ET AL.	257	3	
B.							
C.							
D.							

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	NO
E.							
F.							
G.							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

H.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Jeong, U.I., Jeong, H.S. and Kim, Kinam, "Completely CMOS-Compatible Phase-Change Nonvolatile RAM Using NMOS Cell Transistors," presented at 2003 19 <sup>th</sup> IEEE Non-Volatile Semiconductor Memory Workshop, Monterey, California, February 26-20, 2003
I.	Ha, Y.H., Yi, J.H., Horii, H., Park, J.H., Joo, S.H., Park, S.O., Chung, U-In and Moon, J.T., "An Edge Contact Type Cell for Phase Change RAM Featuring Very Low Power Consumption," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003
J.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Oh, J.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Chung, U.I., Jeong, H.S. and Kim, Kinam, "Full Integration and Reliability Evaluation of Phase-change RAM Based on 0.24 mm-CMOS Technologies," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003
K.	Horii, H., Yi, J.H., Park, J.H., Ha, Y.H., Baek, I.G., Park, S.O., Hwang, Y.N., Lee, S.H., Kim, Y.T., Lee, K.H., Chung, U-In and Moon, J.T., "A Novel Cell Technology Using N-doped GeSbTe Films for Phase Change RAM," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003
L.	Wicker, G.C., "Phase Change Memory and Method Therefor", U.S. Patent Application Serial No. 10/318,984, filed December 13, 2002
M.	Wicker, G.C., "Lateral Phase Change Memory and Method Therefor", U.S. Patent Application Serial No. 10/319,204, filed December 13, 2002
N.	

EXAMINER

DATE CONSIDERED

12/10/04

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.